R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIG. 3 and in the specification as originally filed, for example, on page 7, lines 17-21. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1,3-4,10, 12, 16, 20-22 and 24-25 under 35 U.S.C. §102(b) as being anticipated by Uchida '304 (hereinafter Uchida) has been obviated by appropriate amendment and should be withdrawn.

Uchida is directed to a semiconductor integrated circuit (Title). Uchida describes selecting an identification code for a device via bond optioning bonding pads to a GND pin during assembly (see column 3, line 58 through column 4, line 5 and column 6, lines 14-33 of Uchida). Uchida does not disclose or suggest a circuit configured to generate a plurality of identification codes in response to a logical combination of (i) one or more voltage levels on one or more inputs, (ii) a state of one or more bond options and (iii) a state of one or more metal options, as presently claimed

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(claim 1). Specifically, the Office Action admits that Uchida does not specifically teach generating ID codes in response to a logical combination of (i) one or more voltage levels on one or more inputs, (ii) a state of one or more bond options and (iii) a state of one or more metal options, as presently claimed (see page 8, lines 20-21 of the Office Action). Claims 16 and 20 include similar recitations. Therefore, Uchida does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over Uchida and the rejection should be withdrawn.

Claims 2, 4-15, 17-19 and 21-25 depend, either directly or indirectly, from claims 1 or 16 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the Uchida and the rejections should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 2 and 5-9 under 35 U.S.C. §103(a) as being obvious over Uchida in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 11 and 13-14 under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael et al.

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'311 (hereinafter Carmichael) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 15 under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael and further in view of Werger et al. '246 (hereinafter Werger) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 17 under 35 U.S.C. §103(a) as being obvious over Uchida in view of IBM TDB Publication "Using a portion of the boundary register as the identification register" (hereinafter IBM) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 18-19 under 35 U.S.C. §103(a) as being obvious over Uchida in view of IBM and further in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990) has been obviated by appropriate amendment and should be withdrawn.

Uchida is directed to a semiconductor integrated circuit (Title). Uchida describes selecting an identification code for a device via bond optioning bonding pads to a GND pin during assembly (see column 3, line 58 through column 4, line 5 and column 6, lines 14-33 of Uchida). In contrast, the presently claimed invention (claim 1) provides a circuit configured to generate a plurality of identification codes in response to a logical combination of (i) one or more voltage levels on one or more inputs, (ii) a state of

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one or more bond options and (iii) a state of one or more metal options. Claims 16 and 20 include similar recitations. The Office Action admits that Uchida did not specifically teach generating ID codes in response to a logical combination of (i) one or more voltage levels on said one or more pins, (ii) a state of one or more bond options and (iii) a state of one or more metal options, as presently claimed (see page 8, lines 20-21 of the Office Action).

IBM does not cure the deficiencies of Uchida (as suggested in the last two lines on page 8 of the Office Action). Specifically, IBM is directed to using a portion of the boundary scan register as the identification register (Title). Assuming, arguendo, the ID code bits of IBM are similar to the presently claimed plurality of identification codes, IBM does not teach or suggest each and every element of the presently claimed invention. In particular, IBM states that the ID code bit inputs are hardwired to a logical zero or one level depending upon the value needed for the ID at each bit position in the register (see page 2, lines 8-12 of IBM). Since IBM teaches that each of the ID code bits are hardwired, it follows that the ID code bits of IBM are not generated in response to a logical combination of (i) one or more voltage levels on one or more pins, (ii) a state of one or more bond options and (iii) a state of one or more metal options, as presently claimed. As such, Uchida and IBM, alone or in

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combination, do not teach or suggest each and every element of the presently claimed invention. Therefore, the Office Action does not meet the Offices burden of factually supporting a conclusion of obviousness (see MPEP §2142). As such, the presently claimed invention is fully patentable over the combination of Uchida and IBM and the rejection should be withdrawn.

Furthermore, the position taken in the Office Action that the "Combined Boundary Scan/Device ID Register" in FIG. 4 of IBM teaches generating ID codes in response to a logical combination of (i) one or more voltage levels on one or more pins, (ii) a state of one or more bond options and (iii) a state of one or more metal options, as presently claimed, is not technically correct. Specifically, the Office Action presents no factual evidence or convincing line of reasoning to support the position that the Combined Boundary Scan/Device ID Register is capable of generating a plurality of identification codes in response to a logical combination of (i) one or more voltage levels on one or more pins, (ii) a state of one or more bond options and (iii) a state of one or more metal options, as presently claimed. IBM is silent regarding the register generating a plurality of identification codes in response to a logical combination of (i) one or more voltage levels on one or more pins, (ii) a state of one or more bond options and (iii) a state of one or more metal options, as presently claimed.

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In particular, IBM states that "The ID Code Bits are loaded into the register by CAPTURE ID CLK ..." (page 2, lines 12-14 of IBM, EAST Version). Since the ID Code Bits of IBM are loaded into the register, it follows that the register of IBM does not generate a plurality of identification codes, as presently claimed. One skilled in the art would not view the Combined Boundary Scan/Device ID Register of IBM as being the same as a circuit configured to generate a plurality of identification codes in response to a logical combination of (i) one or more voltage levels on one or more pins, (ii) a state of one or more bond options, and (iii) a state of one or more metal options, as presently claimed. Therefore, the Office Action fails to factually support a conclusion of obviousness (see MPEP §2142). As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Claims 2-15, 17-19 and 21-25 depend, either directly or indirectly, from claims 1 or 16 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.
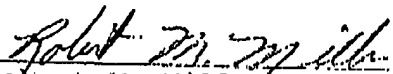
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

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The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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